CLAIMS

1. A hold type image display apparatus comprising:

a panel including a plurality of data lines, a plurality of gate lines, and first and second type pixels located at intersections between said data lines and said gate lines, every one or more of said first type pixels and every one or more of said second type pixels being staggered at said intersections, wherein each of said first type pixels is connected to one of said data lines and two successive ones of said gate lines, and each of said second type pixels is connected to one of said data lines and one of said gate lines;

a gate line driver circuit, connected to said gate lines, for scanning two first successive ones of said gate lines for writing first video data and two second successive ones of said gate lines for writing first black data in a first selection period and for scanning a preceding one of said first successive gate lines for writing second video data and a preceding one of said second successive gate lines for writing second black data in a second selection period; and

a data line driver circuit, connected to said data lines, for supplying said first video data and said first black data to said data lines in said first selection period and for supplying said second video data and said second black data to said data lines in said second selection period.

2. The hold type image display apparatus as set forth in claim 1, wherein each of said first type pixels comprises:

a first pixel capacitor including liquid

crystal; and

first and second thin film transistors connected in series between one of said data lines and said first pixel capacitor, said first and second thin film transistors having respective gates connected to two successive ones of said gate lines,

each of said second type pixels comprising:

a second pixel capacitor including liquid crystal; and

third and fourth thin film transistors connected in series between one of said data lines and said second pixel capacitor, said third and fourth thin film transistors having respective gates connected to one of said gate lines.

3. The hold type image display apparatus as set forth in claim 1, wherein each of said first type pixels comprises:

a first pixel capacitor including liquid crystal; and

first and second thin film transistors connected in series between one of said data lines and said first pixel capacitor, said first and second thin film transistors having respective gates connected to two successive ones of said gate lines,

each of said second type pixels comprising:

a second pixel capacitor including liquid crystal; and

a third thin film transistor connected between one of said data lines and said second pixel capacitor, said third thin film transistor having a gate connected to one of said gate lines,

an ON resistance of said third thin film transistor being equivalent to an ON resistance of said first and second thin film transistors.

4. The hold type image display apparatus as set forth in claim 1, wherein a difference in a number of said gate lines between said two first successive gate lines and said two second successive gate lines is k where k is 1, 3, 5, ···.

5. The hold type image display apparatus as set forth in claim 1, wherein said gate line driver circuit comprises:

first and second shift register circuits for receiving two vertical start pulse signals per one frame period to shift said vertical start pulse signals in synchronization with a vertical clock signal, said first shift register circuit including serially-connected first flip-flops clocked by rising edges of said vertical clock signal to generate first signals, said second shift register circuit including serially-connected second flip-flops clocked by falling edges of said vertical clock signal to generate second signals;

a gate circuit, connected to said first and second shift register circuits, for receiving said first and second signals to generate scanning signals for scanning said two first successive gate lines and said two second successive gate lines; and

an output buffer circuit, connected to said gate circuit, for amplifying said scanning signals.

6. The hold type image display apparatus as set forth in claim 1, wherein said first and second selection periods form one horizontal period,

a sequence of said first video data and

said first black data being opposite to a sequence of said second video data and said second black data.

7. The hold type image display apparatus as set forth in claim 6, wherein polarities of said first video data and said first black data are opposite to those of said second video data and said second black data.

8. The hold type image display apparatus as set forth in claim 1, wherein said data line driver circuit comprises:

a shift register circuit for receiving two horizontal start pulse signals per one horizontal period to shift said two horizontal start pulse signals in synchronization with a horizontal clock signal, said shift register circuit including serially-connected third flip-flops clocked by said horizontal clock signal to generate latch signals, the number of said third flip-flops being half of the number of said data lines;

a data register circuit, connected to said shift register circuit, for latching said first and second video data in synchronization with said latch signals;

a digital/analog conversion circuit, connected to said data register circuit, for performing digital/analog conversions upon said first and second video data latched in said data register circuit;

a black data voltage generation circuit for generating at least one black data; and

an output buffer circuit, connected to said digital/analog conversion circuit and said black data voltage generation circuit, for multiplexing and supplying said first and second video data and said black data to said data lines.

9. The hold type image display apparatus as set

forth in claim 8, wherein said output buffer circuit includes a plurality of amplifiers for amplifying said analog first and second video data voltages, the number of said amplifiers being half of the number of said data lines.

10. The hold type image display apparatus as set forth in claim 8, wherein every one of said first type pixels and every one of said second type pixels are staggered at said intersections between said data lines and said gate lines,

said digital/analog conversion circuit comprising:

a plurality of positive side digital/analog converters;

a plurality of negative side digital/analog converters; and

multiplexers, connected to said positive side digital/analog converters and said negative side digital/analog converters, for selecting said positive side digital/analog converters or said negative side digital/analog converters in accordance with a polarity signal,

said black data voltage generation circuit selecting and generating negative side black data or positive side black data in accordance with said polarity signal.

11. The hold type image display apparatus as set forth in claim 10, wherein said output buffer circuit comprises a plurality of muliplexers, each connected to said digital/analog conversion circuit, said black data voltage generation circuit and two of said data line, for multiplexing said first and second video signals and said black data.

12. The hold type image display apparatus as set forth in claim 8, wherein every two of said type pixels and every two of said second type pixels are staggered at said intersections between said data lines and said gate lines,

said digital/analog conversion circuit comprising:

a plurality of positive side digital/analog converters;

a plurality of negative side digital/analog converters; and

multiplexers, connected to said positive side digital/analog converters and said negative side digital/analog converters, for multiplexing said positive side digital/analog converters and said negative side digital/analog converters in accordance with a polarity signal,

said black data voltage generation circuit multiplexing positive side black data and negative side black data in accordance with said polarity signal.

13. The hold type image display apparatus as set forth in claim 12, wherein said output buffer circuit comprises a plurality of muliplexers, each connected to said digital/analog conversion circuit, said black data voltage generation circuit and four of said data line, for multiplexing said first and second video signals and said black data.

14. A panel used in a hold type image display apparatus, comprising:

a plurality of data lines;

a plurality of gate lines; and

first and second type pixels located at

intersections between said data lines and said gate lines, every one or more of said first type pixels and every one or more of said second type pixels being staggered at said intersections, wherein each of said first type pixels is connected to one of said data lines and two successive ones of said gate lines, and each of said second type pixels is connected to one of said data lines and one of said gate lines.

15. The panel as set forth in claim 14, wherein each of said first type pixels comprises:

a first pixel capacitor including liquid crystal; and

first and second thin film transistor connected in series between one of said data lines and said first pixel capacitor, said first and second thin film transistors having respective gates connected to two successive ones of said gate lines,

each of said second type pixels comprising:

a second pixel capacitor including liquid crystal; and

third and fourth thin film transistors connected in series between one of said data lines and said second pixel capacitor, said third and fourth thin film transistors having respective gates connected to one of said gate lines.

16. The panel as set forth in claim 14, wherein each of said first type pixels comprises:

a first pixel capacitor including liquid crystal; and

first and second thin film transistors connected in series between one of said data lines and said first pixel capacitor, said first and second thin

film transistors having respective gates connected to two successive ones of said gate lines,

each of said second type pixels comprising:

a second pixel capacitor including liquid crystal; and

a third thin film transistor connected between one of said data lines and said second pixel capacitor, said third thin film transistor having a gate connected to one of said gate lines,

an ON resistance of said third thin film transistor being equivalent to an ON resistance of said first and second thin film transistors.

17. A gate line driver circuit used in a hold type image display apparatus including a panel formed by a plurality of data lines, a plurality of gate lines, and first and second type pixels located at intersections between said data lines and said gate lines, every one or more of said first type pixels and every one or more of said second type pixels being staggered at said intersections, each of said first type pixels being connected to one of said data lines and two successive ones of said gate lines, each of said second type pixels being connected to one of said data lines and one of said gate lines,

wherein said gate line driver circuit scans two first successive ones of said gate lines for writing first video data and two second successive ones of said gate lines for writing first black data in a first selection period and scans a preceding one of said first successive gate lines for writing second video data and a preceding one of said second successive gate lines for writing second black data in a second selection period.

18. The gate line driver circuit as set forth in claim 17, wherein a difference in a number of said gate lines between said two first successive gate lines and said two second successive gate lines is k where k is 1, 3, 5, ….

19. The gate line driver circuit as set forth in claim 17, comprising:

first and second shift register circuits for receiving two vertical start pulse signals per one frame period to shift said vertical start pulse signals in synchronization with a vertical clock signal, said first shift register circuit including serially-connected first flip-flops clocked by rising edges of said vertical clock signal to generate first signals, said second shift register circuit including serially-connected second flip-flops clocked by falling edges of said vertical clock signal to generate second signals;

a gate circuit, connected to said first and second shift registers, for receiving said first and second signals to generate scanning signals for scanning said two first successive gate lines and said two second successive gate lines; and

an output buffer circuit, connected to said gate circuit, for amplifying said scanning signals.

20. A data line driver circuit used in a hold type image display apparatus including a panel formed by a plurality of data lines, a plurality of gate lines, and first and second type pixels located at intersections between said data lines and said gate lines, every one or more of said first type pixels and every one or more of said second type pixels being staggered at said intersections, each of said first type pixels being

connected to one of said data lines and two successive ones of said gate lines, each of said second type pixels being connected to one of said data lines and one of said gate lines,

wherein said data line driver circuit supplies first video data and first black data to said data lines in a first selection period and supplies second video data and second black data to said data lines in a second selection period.

21. The data line driver circuit as set forth in claim 20, wherein said first and second selection periods form one horizontal period,

a sequence of said first video data and said first black data being opposite to a sequence of said second video data and said second black data.

22. The data line driver circuit as set forth in claim 21, wherein polarities of said first video data and said first black data are opposite to those of said second video data and said second black data.

23. The data line driver circuit as set forth in claim 20, comprising:

a shift register circuit for receiving two horizontal start pulse signals per one horizontal period to shift said two horizontal start pulse signals in synchronization with a horizontal clock signal, said shift register circuit including serially-connected third flip-flops clocked by said horizontal clock signal to generate latch signals, the number of said third flip-flops being half of the number of said data lines;

a data register circuit, connected to said shift register circuit, for latching said first and second video data in synchronization with said latch signals;

a digital/analog conversion circuit, connected to said data register circuit, for performing digital/analog conversions upon said first and second video data latched in said data register circuit;

a black data voltage generation circuit for generating at least one black data; and

an output buffer circuit, connected to said digital/analog conversion circuit and said black data voltage generation circuit, for multiplexing and supplying said first and second video data and said black data to said data lines.

24. The data line driver circuit as set forth in claim 23, wherein said output buffer circuit includes a plurality of amplifiers for amplifying said analog first and second video data voltages, the number of said amplifiers being half of the number of said data lines.

25. The data line driver circuit as set forth in claim 23, wherein every one of said first type pixels and every one of said second type pixels are staggered at said intersections between said data lines and said gate lines,

said digital/analog conversion circuit comprising:

a plurality of positive side digital/analog converters;

a plurality of negative side digital/analog converters; and

multiplexers, connected to said positive side digital/analog converters and said negative side digital/analog converters, for selecting said positive side digital/analog converters or said negative side digital/analog converters in accordance with a polarity signal,

said black data voltage generation circuit selecting and generating negative side black data or positive side black data in accordance with said polarity signal.

26. The data line driver circuit as set forth in claim 25, wherein said output buffer circuit comprises a plurality of muliplexers, each connected to said digital/analog conversion circuit, said black data voltage generation circuit and two of said data line, for multiplexing said first and second video signal and said black data.

27. The data line driver circuit as set forth in claim 23, wherein every two of said first type pixels and every two of said second type pixels are staggered at said intersections between said data lines and said gate lines,

said digital/analog conversion circuit comprising:

a plurality of positive side digital/analog converters;

a plurality of negative side digital/analog converters; and

multiplexers, connected to said positive side digital/analog converters and said negative side digital/analog converters, for multiplexing said positive side digital/analog converters and said negative side digital/analog converters in accordance with a polarity signal,

said black data voltage generation circuit multiplexing negative side black data or positive side black data in accordance with said polarity signal.

28. The data line driver circuit as set forth in

claim 27, wherein said output buffer circuit comprises a plurality of muliplexers, each connected to said digital/analog conversion circuit, said black data voltage generation circuit and four of said data line, for multiplexing said first and second video signal and said black data.

29. A method for driving a hold type image display apparatus comprising: a panel including a plurality of data lines, a plurality of gate lines, and first and second type pixels located at intersections between said data lines and said gate lines, every one or more of said first type pixels and every one or more of said second type pixels being staggered at said intersections, wherein each of said first type pixels is connected to one of said data lines and two successive ones of said gate lines, and each of said second type pixels is connected to one of said data lines and one of said gate lines, said method comprising:

scanning two first successive ones of said gate lines for writing first video data and two second successive ones of said gate lines for writing first black data in a first selection period;

supplying said first video data and said first black data to said data lines in said first selection period;

scanning a preceding one of said first successive gate lines for writing second video data and a preceding one of said second successive gate lines for writing second black data in a second selection period; and

supplying said second video data and said second black data to said data lines in said second selection period.

30. The method as set forth in claim 29, wherein a difference in a number of said gate lines between said two first successive gate lines and said two second successive gate lines is k where k is 1, 3, 5, ···.

31. The method as set forth in claim 29, wherein said scanning comprises:

receiving two vertical start pulse signals per one frame period to shift said vertical start pulse signals in synchronization with a vertical clock signal, to generate first signals and second signals;

receiving said first and second signals to generate scanning signals for scanning said two first successive gate lines and said two second successive gate lines; and

amplifying said scanning signals.

32. The method as set forth in claim 29, wherein said first and second selection periods form one horizontal period,

a sequence of said first video data and said first black data being opposite to a sequence of said second video data and said second black data.

33. The method as set forth in claim 32, wherein polarities of said first video data and said first black data are opposite to those of said second video data and said second black data.

34. The method as set forth in claim 29, wherein said supplying comprises:

receiving two horizontal start pulse signals per one horizontal period to shift said two horizontal start pulse signals in synchronization with a horizontal clock signal;

latching said first and second video data in synchronization with said latch signals;

performing digital/analog conversions upon said latched first and second video data;

generating at least one black data; and

multiplexing and supplying said first and second video data and said black data to said data lines.

35. The method as set forth in claim 34, wherein every one of said first type pixels and every one of said second type pixels are staggered at said intersections between said data lines and said gate lines,

said digital/analog performing comprising:

selecting a positive side digital/analog performing or a negative side digital/analog performing in accordance with a polarity signal; and

selecting and generating negative side black data or positive side black data in accordance with said polarity signal.

36. The method as set forth in claim 34, wherein every two of said first type pixels and every two of said second type pixels are staggered at said intersections between said data lines and said gate lines,

said digital/analog performing comprising:

multiplexing a positive side digital/analog performing and a negative side digital/analog performing in accordance with a polarity signal; and

multiplexing negative side black data or positive side black data in accordance with said polarity signal.